Real Time System for Image Acquisition and Pattern Recognition Using Boolean Neural Network

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Abstract: *The system presented in this paper consists of an image acquisition module from a video camera, an image processing module, which performs conversion to monochrome format, and a neural network that takes the acquired images and performs the extraction of patterns from them. The system proposed by the authors is used for recognizing the orientation of objects in real time by analyzing images from a common video camera. The acquisition module is based on three high–speed AD converters. The remaining components: the digital image processor and the neural network used to classify the shapes of objects are both integrated into a FPGA circuit. All these ensure integration in one chip and a high speed response – typical requirements for a real–time system.*

1. INTRODUCTION

Working with FPGA circuits requires knowledge of hardware description languages and techniques of digital circuits design. The appearance of FPGA circuits had revolutionized the design of intelligent algorithms. The concept of these new algorithms is based on performing parallel computing rather than sequential processing.

In general, the artificial intelligence algorithms are used to solve problems difficult to treat by conventional methods. There are three major classes of algorithms: neural networks, evolutionary algorithms and fuzzy calculation used in all fields [1]. Being pseudo random solutions is difficult to determine response time; it varies even with the same input data. In their conventional form (that can be implemented into a computer program) they cannot be used as real time response solutions.

By implementing hardware and using parallel component modules it can reduce the learning time to allow a real time response. Thus, more and more applications can use reconfigurable circuits for real-time response [2].

Artificial neural networks can be implemented using hardware parallel modules in more efficient ways, in terms of the rate of learning and testing [3].

There are many techniques presented for hardware implementation of the neural networks, some of these being treated in recent work papers: digital circuits [4], optical [5] and analog circuits [6]. Our solution of hardware neural network consists in using a Boolean artificial neural network (ANN) implemented in a FPGA circuit. In our case, Boolean ANN permits to recognize the pattern extracted from the image. Extraction of the pattern from image obtained from a camera (the kind used in security equipment) is possible through mid-level image processing. The obtained monochrome image is applied to the network's input. The objects in the image are extracted and then classified.

The paper is divided into several sections. Next section deals with the presentation of capture and image conversion. Image capture is made with an AD converter from Analog Device from a VDEC board. It contains a high speed Hirose connector that can make possible interfacing with the main system (FPGA). VDEC board is used to convert the image taken in analogue format, in digital form, in order to be introduced in recognition stage, via a module implemented in FPGA.

Section 3 of article presents artificial neural network built for reconnaissance. It went on a binary neural network model (inclusive with weights in binary). The experimental board is shown in Section 4. The results

are presented and related to resource allocation in FPGA and the response time of the system.

2. IMAGE CONVERSION MODULE

In the figure below is shown a block diagram of the acquisition and image processing module, fully integrated in the FPGA.

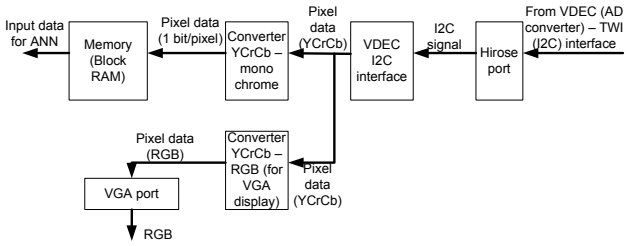

Fig. 1. Image acquisition module. We used a conventional image processing module: conversion from AD output, YCrCb to monochrome conversion then memory of the frame (image).

The image taken by video camera is applied to the high speed AD converter of the VDEC board. The AD converter works at a frequency of 80 MHz and it converts in digital format each pixel received from video camera, providing 16 serial bit data.

Data is transmitted through a synchronous serial interface (two wire interface through high-speed Hirose connector).

The first module built into the FPGA ensures conversion of serial data format in parallel YCrCb format (for every pixel). In the next stages, there are two converters: from YCrCb in monochrome format - that will generate the image needed to be processed by the neural network and in RGB format, that will generate the required image to be output of a VGA port for a local monitor (for control). Monochrome image is stored in a bi-port memory to be then provided to artificial neural network.

3. BOOLEAN ARTIFICIAL NEURAL NETWORK MODULE

The figure below provides a block diagram of recognize shapes module, based on the analysis of ANN. As can be seen in the figure, from the BRAM memory where are stored all the bits of a monochrome image, the information reaches the artificial neural network. Along with the image memory, there is a pattern memory (which is initialized with the appropriate patterns from the circuit synthesis stage). Patterns memory is used in the training phase of the network. The patterns counter is controlled by error evaluation module.

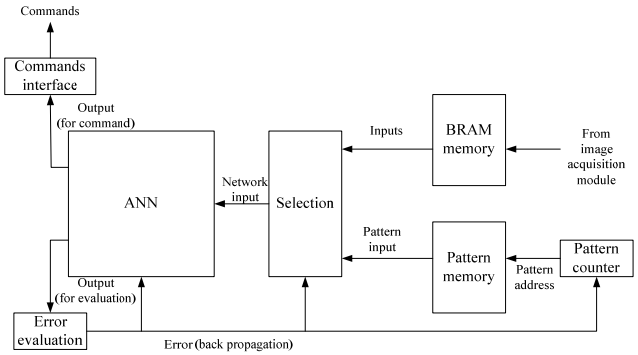

Fig. 2. Object recognition module. The main component is ANN module which is used to recognize objects from image stored in BRAM memory.

It compares, during learning, the expected output specified in the template with the obtained output. The selection circuit allows choosing the operating mode of the network: learning (training) or test (shapes recognition). We designed an artificial neural network (Boolean), and feed-forward back-propagation learning algorithm.

The structure of a binary neural network is shown in Figure 3. Binary neural networks are characterized by binary values (0 or 1) for the neurons and all weights. To compensate the limited field of binary values (only 0 and 1) a special procedure is performed to generate pseudo-random weights.

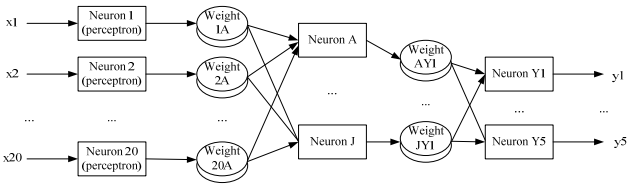

Fig. 3. Neural network (20-10-5) block diagram. In our solution weights are stored in finite state machines with pseudo-random transitions activation.

In order to achieve diversity in the values of weights were used finite states machines (FSM) for which the transition takes place depending to error, but according to a pseudo random sequence. The structure of such a control is shown in Figure 4. Output of a weight FSM is always 0 or 1. The command output may take values as stated by following entries: the state of the neuron connected to the weight module, the error status that comes from

the network output or the "rand" entry – connected to a pseudo-random sequence generator.

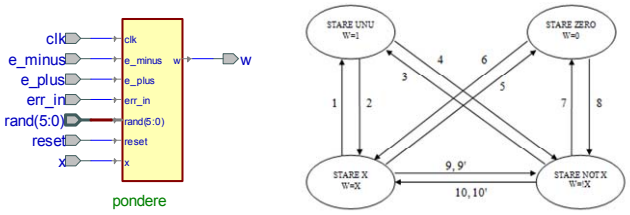

Fig. 4. Weight finite state machine. Output w can be only 1 or 0. The machine has 4 states, 2 for w=1 and 2 for w=0. Transition between states is performed by events on error inputs (inputs with e) and events on random input (from RNG).

4. Experimental System and Results

A block diagram of the system is shown in Figure 5. The system is intended for monitoring and correctly positioning of parts on an assembling line. This requires detecting the currently position of the part. The job is done using images from a video camera (usually used in security) that are captured and processed with Boolean ANN. The special feature in our application is the real-time response of the system. ANN configuration is presented in table below:

Tab. 1. ANN configuration used.

Size	Value
Number of networks	4
Input neurons (perceptron)	25
Hide layer	10
Output layer	5
Weight modules input-hide layer	250
Weight modules hide-output layer	50

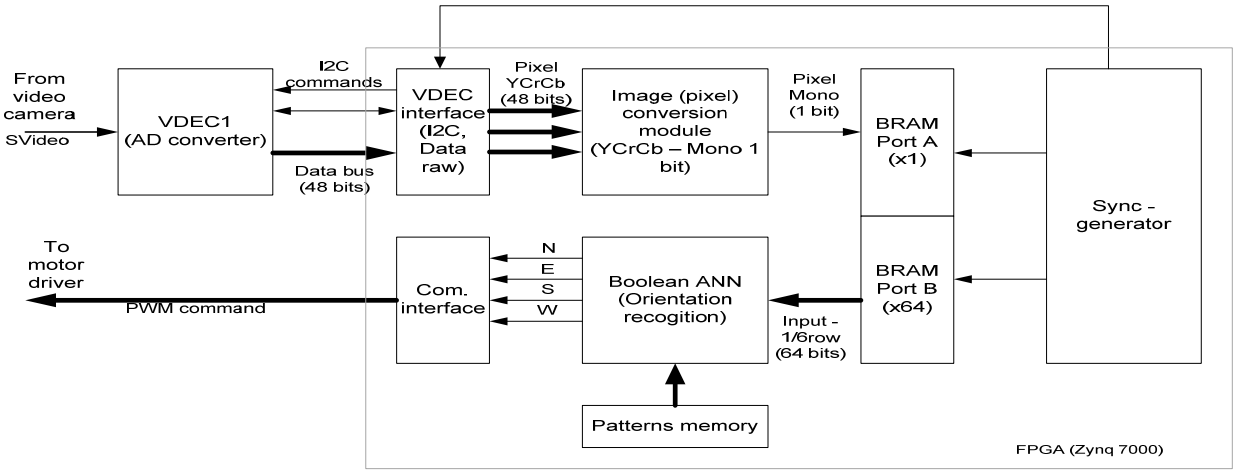

Fig. 5. Block diagram of acquisition system. Dual port RAM is used to store pixel information (port A) and read monochrome information from pixels (Port B).

Figure 6 presents a block diagram of the system. Extracting image, converting it from YCbCr format 4:2:2 to monochrome and storing of the result is done by the FPGA circuit at converter's acquisition rate. One port from a bi-port Block RAM memory (BRAM) inside FPGA is used for storing mechanism. The other port of BRAM is used by the Boolean neural network that takes the image and classifies patterns from it. The performances of our proposed system are expected to be at a higher level having in mind the strength of the parallel implementation for neural networks which involve less processing time.

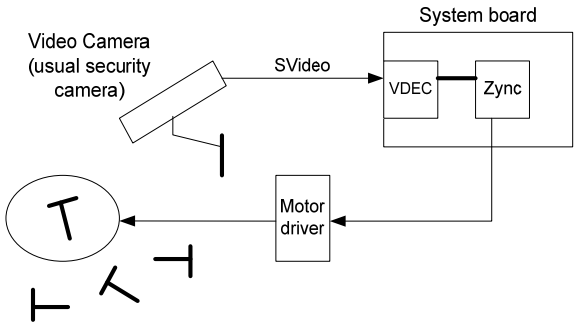

Fig. 6. Application block diagram. Images (frames) are taken from usual security video camera, then are processed in real time with a FPGA based system.

Tab. 2. Image configuration.

Size	Value
Resolution of image from video camera	400x300
Resolution of image stored in BRAM memory	10x10
Resolution for logical pixel used as input in ANN	40x30
AD frequency	80MHz
AD data size	16 bits

As can be seen in Table 3, takes longer to read a pixel (information Y, Cr and Cb 16 bits each): 480 us; compared to the processing in FPGA (which in total reach 18 ns). Convergence time of 300 ms is applied only at the beginning stage of learning.

Tab. 3. Resources used and response time.

Size	Value
Logic allocated inside FPGA (including acquisition module)	~50% neural network (~12.5% Slices allocated for one neural network) 13% resources for acquisition TOTAL 63%
Convergence time (learning time)	Max. 300 ms
Normal operation response time (including acquisition module)	~12 ns delay path in neural network 6 ns delay path for acquisition module TOTAL 18ns
Clock frequency for I2C read	100kHz
1 pixel read time (from VDEC circuit)	48 x 10 us = 480 us

5. CONCLUSIONS

As can be seen from the results, even network training phase takes less than one second. Instead, the testing regime, the system can identify the position of a track in less than 1 ms by image analysis from an ordinary camera. The entire application – except the AD converter of course – is integrated into a single FPGA. The entire application – except the AD converter and of course video camera – is integrated into a single FPGA.

The novelty brought is to integrate the whole application (unlike other solutions using computer image analysis) and the ability to respond in real time. Future research directions are related to the extension of other types of data extraction from image.

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